WHAT IS CLAIMED IS:

1. A video signal processing apparatus comprising:

a detector which detects whether or not an input video signal is based on a telecine-converted video signal obtained by telecine conversion in a 2-3 pulldown conversion system from a film source having 24 film frames per second;

a frame memory;

a writing device which writes the input video signal in said frame memory on a line sequential scanning frame unit base in synchronism with a first vertical synchronizing signal for writing;

a reading device which reads out the written line sequential scanning video signal in said frame memory in synchronism with a second vertical synchronizing signal for reading; and

a synchronism controller which generates the second vertical synchronizing signal having a frequency different from a frequency of the first vertical synchronizing signal in synchronism with the first vertical synchronizing signal of a starting frame of five frames forming a pattern after the conversion in the 2-3 pulldown conversion system when said detector judges that the input video signal is based on a telecine-converted video signal.

2. The video signal processing apparatus according to Claim 1, further comprising a line sequential scanning converter, when the input video signal is an interlaced scanning video signal, which converts the interlaced scanning video signal

into a line sequential scanning video signal to supply the line sequential scanning video signal to said frame memory,

wherein said detector detects whether or not the input video signal is based on said telecine-converted video signal in accordance with the interlaced scanning video signal.

3. The video signal processing apparatus according to Claim 1, further comprising a synchronism detector which detects a vertical synchronizing signal in the video signal supplied to said frame memory to generate the first vertical synchronizing signal.

4. The video signal processing apparatus according to Claim 1, wherein the different frequency is 6/5 of the frequency of the first vertical synchronizing signal, and wherein said synchronism controller generates the second vertical synchronizing signal by six times in a period of five cycles of the first vertical synchronizing signal.